REMARKS

The Office Action

Claims 1-16 were presented for examination. Claims 1 and 3 stand rejected as being indefinite, as the Examiner stated it was not clear what "hfe" was intended to represent.

All claims (1-16) are all now presently rejected as being anticipated by the reference Nilssen ('915).

The Non-Art Objections and Rejections

Applicants have amended Figures 5 and 6 to be designated as Figures 5a and 5b, and Figures 6a and 6b, respectively. This change is shown in the attached Request for Amendment to Drawings.

The Examiner proposed all numerical designation such as "[0001]" to "[0023]" should be deleted. Applicant respectfully requests the Examiner reconsider this position. This application was filed in accordance with electronic filing procedures, and it is respectfully submitted the numerical designations on the left border of each page are appropriate.

Amendments to the brief description of the drawings have been made in accordance with the amendment to the Figures, and the Examiner's observations.

Turning attention to claims 3 and 10, it is submitted these claims are appropriate under 35 U.S.C. § 112, second paragraph.

Particularly, the term "hfe" refers to an industry standard term for the DC gain or beta of a transistor. This hfe designation is found on substantially all transistor data sheets. For the Examiner's records, applicant provides Attachment A, which includes relevant pages 121-123 from a student textbook *Electronic Principles* (Second Edition Malvino Copyright 1979) referencing this standard nomenclature. Also, in the specification in paragraph [0014], the fourth and fifth lines from the bottom of that paragraph, it is noted the circuit of an embodiment in the present invention is configured with switches 40 and 42 having mismatched hfe's (commonly called beta). It is this mismatching which causes a transistor with a lower hfe to conduct for a shorter period of time, which in turn permits the on time of the switches and therefor the output signal to

be asymmetrical. Thus, in one embodiment of the application, the asymmetrical output signal to the load is obtained by using these mismatched transistors. It is to be noted that in an embodiment related to MOSFET switches (for example FIGURE 7), the asymmetrical operation of the MOSFETs which produce the asymmetrical output signal is obtained by the use of the gate voltage limiting zener diodes 98 and 100 having unequal voltage rates.

For these reasons, it is respectfully submitted claims 3 and 10 are distinguished. While the reference supplied to the Examiner indicates that it is more normal to use the designation h_{FE}. Applicant does not believe this is required. However, in order to override this designation in a more standard conformance in the industry, applicant has made such an amendment. It is to understood that this amendment is in no way intended to be limiting or to change the scope of the claims 3 and 10, but rather simply correct typographical issues.

The Art Rejections

Applicant has now had an opportunity to carefully consider the Examiner's application of Nilssen ('915) in the rejection of claims 1-16.

By way of review, Nilssen is directed to an electronic ballast for instant-start lamps. In this ballast, a full-bridge inverter is powered from a DC voltage and provides a square-wave-like inverter output voltage. This inverter output voltage which has a peak amplitude equal to the magnitude of the DC voltage, is applied to an instant-start fluorescent via a current-limiting inductor connected in series with a DC blocking capacitor.

In Nilssen, switches (FET1 and FET2) of the inverter circuit are operated in an alternating fashion to generate the output signal of the inverter. In reviewing the various signals generated by the circuit of Nilssen (*i.e.*, Figs. 3A-3D, 11A-11H, and 15), all signals generated by the inverter are symmetrical. More specifically, nowhere in Nilssen is there a discussion of having the on times and off times of the FET1 and FET2 being designed to be unequal.

Particularly, Figs. 11A, 11E and 11G which show the waveform of a voltage provided at the output of the half-bridge inverter of Fig. 9 for various situations are all

symmetrical. Similarly, Fig. 11D shows current flowing through fluorescent lamps FL1 and FL2 is also symmetrical.

Therefore, Nilssen, which is interested in a ballast for instant-start lamps, has no consideration of the concepts directed to what is claimed in the present application.

More particularly, the present application is concerned with elimination of striations which occur in linear lamps. Applicant had determined that by providing an asymmetrical, alternating current to the lamp, these striations may be eliminated or greatly reduced. To accomplish this result, the present application teaches embodiments for ballasts which provide an asymmetrical output signal. This concept is specifically recited in independent claim 1 where it notes that the inverter circuit is configured to generate an asymmetric alternating current on a lamp input line. While the Examiner recites that Nilssen shows such an inverter circuit, applicant submits that the asymmetric concepts as claimed in claim 1 are not taught or fairly suggested by Nilssen. Dependent claims 2 and 3 further define that the inverter is formed of bipolar junction transistors which are configured to have unequal on-times, and that these unequal on-times may be obtained by having the bipolar junction transistors configured to have unequal h_{FE} values.

A further alternative embodiment of the inverter circuit is defined in claims 4, 5 and 6 to use MOSFET transistor switches, where a back-to-back series connected zener diodes configured with unequal voltage values from each other are used.

Claim 7 defines that a DC blocking capacitor is used to block the DC current from the asymmetric alternating current.

To more particularly emphasize the distinctions which exist between Nilssen and the concepts claimed in the present application, attention is directed to FIGURES 5a, 5b and FIGURES 6a, 6b and the discussion in paragraphs [0015]-[0019] of the present application.

FIGURES 5a and 6a are directed to prior art symmetrical excitation of a resonant load. As noted, waveform 92 shows equal positive and negative durations and equal positive and negative amplitudes. However, in FIGURES 5b and 6b, the asymmetrical load current 90, which is measured as the current flowing from node 54 to node 52 in FIGURE 4, illustrates that the positive portion of the asymmetrical current cycle is of a shorter duration than the negative portion of the cycle. It may further be seen that the

positive portion is of a higher amplitude than the negative portion. Thus, waveform 90 is an asymmetrical load current being supplied to the lamp in order to eliminate the striations which may otherwise occur in the lamp.

For the foregoing reasons, it is submitted independent claim 1 and its dependent claims 2-7 are distinguished from Nilssen ('915).

Turning to independent claim 8 and its dependent claims 9-14, as well as independent claim 15 and its dependent claim 16, these claims also include the above-noted distinguishing concepts from the cited Nilssen patent. Particularly, claim 8 describes a method of generating this asymmetric alternating current to a gas discharge lamp, and independent claim 15 discloses an alternative description of an apparatus for such operation. For these reasons, it is submitted independent claims 8 and 15, as well as their corresponding claims 9-14 and 16, are also distinguished.

Applicant would note that they have amended dependent claims 3 and 10 simply to correct a typographical issue. Claims 6 and 13 have been amended to more particularly clarify that the zener diodes, which are configured with unequal voltage values, are configured with unequal voltage values with relationship to each other. It is submitted this amendment simply clarifies what is inherent in the description.

Applicant has reviewed the additional art cited but not applied. As this art is not deemed any more relevant than the applied art, applicant will not burden the record with a further discussion of this art.

CONCLUSION

For the reasons detailed above, it is respectfully submitted all claims remaining in the application are now in condition for allowance. An early notice to that effect is therefore earnestly solicited.

Respectfully submitted,

FAY, SHARPE, FAGAN,
MINNICH & McKEE, LLP

Mark S. Svat
Reg. No. 34,261
1100 Superior Avenue, 7th Floor
Cleveland, Ohio 44114-2518
(216) 861-5582

Attachments: Excerpt from *Electronic Principles*
(Second Edition Malvino Copyright 1979)

Version with Markings to Show Changes Made

CERTIFICATE OF MAILING

I hereby certify that this Amendment A is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231, on **February 1, 2002.**

By _____
Karen M. Forsyth

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

Please amend pending paragraph [0008] as follows:

[0008] FIGURE 1 illustrates a typical fluorescent lamp having striation zones creating a strobing effect to an end user;

FIGURE 2 illustrates a standing pressure wave in a closed organ pipe;

FIGURE 3 depicts a high-level view of a system implementing the concepts of the present invention;

FIGURE 4 illustrates a preferred embodiment of the present invention;

FIGURE 5a shows a standard forcing function which may be obtained by a prior art system;

FIGURE 5b depicts an input forcing function obtained by use of the concepts of the present invention [compared to a standard forcing function];

FIGURE 6a shows a standard lamp input current;

FIGURE 6b depicts a lamp input current obtained by use of the concepts of the present invention [compared to a standard lamp input current]; and

FIGURE 7 illustrates an alternate embodiment of the present invention.

Please amend pending paragraph [0012] as follows:

[0012] Using this hypothesis, it has been determined that striations in a lamp can be reduced or eliminated by operating a ballast having an inverter at other than a 50% duty ratio. That is, in a two switch inverter, for example, one switch is configured to operate longer than the remaining switch. As long as this offset in the duty ratio is blocked, such as by a capacitor, no DC current will flow through the [lamp"s] lamp's arc. Rather, for example, the positive portion of the of the lamp current cycle will have a shorter duration but a higher amplitude than the succeeding negative portion of the cycle, or vice versa. Consequently, a ballast circuit has been developed which provides an asymmetric input current to the lamp. By

altering the symmetry of the current in this manner, the repetitive resonance frequencies which are believed to create the striations are interfered with thereby eliminating the visual appearance of striations.

Please amend pending paragraph [0013] as follows:

[0013] FIGURE **3** sets forth an exemplary lamp lighting system **20** which incorporates the concepts of the present invention. An input power source **22** supplies power to a ballast **24**. Ballast **24** includes an AC-to-DC converter **26** which provides a DC voltage on DC bus **28** which, in turn, provides power to a lamp input current generating circuit **30**. The lamp input current generating circuit **30** is configured to generate an asymmetric alternating current on lamp input line **32** that provides power to gas discharge lamp **34**. In one embodiment, the lamp input current generating circuit **30** can be an inverter circuit or portions of the inverter circuit, and will be described primarily with this focus. However, it is to be appreciated that other components and circuits capable of generating or supplying an [asymmetric] a symmetric alternating current to lamp **34** may also be used. These additional circuits, which may be represented by block **30** of FIGURE 3, may or may not be part of the inverting circuit. For example, a sub-circuit subsequent to the inverting mechanism can be used to alter asymmetric generated signal into an asymmetric form.

Please amend pending paragraph [0014] as follows:

Set forth in FIGURE 4 is one embodiment of inverter circuit **30** suitable for incorporating concepts of the present invention. Inverting circuits of this type are well known in the industry and, therefore, the circuit will not be described in great detail except where concepts of the present invention are implemented. The circuit comprises complementary switches **40** and **42**, bipolar junction transistors in this exemplary embodiment. The emitters of switches **40** and **42** are connected in common to a series configured resonant circuit **44** including capacitor **46** and inductor **48**. A blocking capacitor **50** is connected to the remaining end of resonant circuit **44** and is series connected to lamp **34** at node **52** with the remaining end of lamp **34** connected to the junction of capacitor **46** and inductor **48** at node **54**. A feedback inductor **56**, a tap from

inductor **48**, is connected to the common emitters of switches **40** and **42** at node **58** with the remaining end of inductor **56** series connected to driving inductor **60** which is connected, in turn to feedback capacitor **62**. The remaining end of feedback capacitor **62** is connected to the base terminals of switches **40** and **42**. A first resistor **64** is connected from the base terminals of switches **40** and **42** to the collector terminal of switch **40** which is also connected to the positive lead of DC bus **28** at node **66**. The collector terminal of switch **42** is connected to ground **68** which is connected to the negative lead of DC bus **28** at node **70**. Driving inductor **60** is bridged by output clamping circuit **72** comprising back-to-back, series connected zener diodes **74** and **76**. Capacitor **78** bridges resonant circuit **44**, and resistor **80** is connected between node **58** and ground **68**. Reverse-conducting diode **82** bridges the emitter and collector terminals of switch **40**, with the cathode of diode **82** connected to the collector terminal of switch **40**. Reverse-conducting diode **84** bridges the emitter and collector terminals of switch **42**, with the anode of diode **84** connected to the collector terminal of switch **42**. A preferred method of producing asymmetry in the lamp input current for the circuit illustrated in FIGURE 4 is to configure switches **40** and **42** with mismatched [hfe] $\underline{h_{FE}}$ (commonly called beta). This causes the transistor with a lower [hfe] $\underline{h_{FE}}$ to conduct for a shorter period of time, thereby causing the on time of switches **40** and **42** to be asymmetrical. That is, one BJT will conduct for a shorter period of time than the other will.

Please amend pending paragraph [0015] as follows:

[0015] FIGURE 5b shows an asymmetrical forcing function **86** of the present invention compared to a typical symmetrical forcing function **88** of FIGURE 5a of prior art ballast inverters. The forcing function is a voltage as measured from node **58** with respect to node **52** in FIGURE 4. The particular forcing function shown is configured to have a short positive duration and a long negative duration. The positive and negative durations can be reversed with equal efficacy.

Please amend pending paragraph [0016] as follows:

[0016] FIGURE 6b illustrates the effect of asymmetrical forcing function **86**. Asymmetrical load current **90**, measured as the current flowing from node **54** to node **52**

[is shown in the lower half of FIGURE 5], and can be compared to a symmetrical load current **92** shown in [the upper half of] FIGURE 6a. The positive portion of the asymmetrical current cycle is of shorter duration than the negative portion of the cycle, however, the positive portion is of a higher amplitude than the negative portion. Symmetrical load current **92**, however, shows equal positive and negative durations, and equal positive and negative amplitudes. There is no DC component to asymmetrical load current **90** because DC current is blocked by blocking capacitor **50**.

Please amend pending paragraph [0018] as follows:

[0018] In a prior art inverter incorporating complementary MOSFET switches, voltage-limiting zeners **98** and **100** would be configured with equal component voltage ratings. However, in this alternate embodiment of the present invention, zener diodes **98** and **100** are configured with unequal voltage ratings. The unequal voltage ratings cause one of switches **94** and **96** to be in an on state longer than the opposite switch. The effect of unequal on times of switches **94** and **96** will be the same as illustrated in FIGURES 5a-5b and 6a-6b for BJT switches **40** and **42**.

In the Claims

Please amend claims 3, 6, 10 and 13 as follows:

3. (Amended) The ballast circuit according to claim 2 wherein the bipolar junction transistor switches are configured to have unequal [hfe] h_{FE} values.

6. (Amended) The ballast circuit according to claim 5 wherein the Zener diodes are configured with unequal voltage values from each other.

10. (Amended) The method according to claim 9 wherein the bipolar junction transistor switches are configured to have unequal [hfe] h_{FE} values.

13. (Amended) The method according to claim 12 wherein the Zener diodes

are configured with unequal voltage values from each other.